Page 4, line 11	After "generation.", insert --FIG. 7 depicts an illustrative timing relationship of the signals used for gray scale control including a frame time, a plurality of LOAD and ILLUMINATE periods, a drive current, data signals, a linear ramp control signal and a stepped control signal.--; and
Page 4, line 48	After "period.", insert --FIG. 8 depicts an illustrative timing relationship of the signals used for digital gray scale control including a frame time, a plurality of LOAD and ILLUMINATE periods, a drive current, data signals, a linear ramp control signal and a stepped control signal.--.

IN THE CLAIMS

Please amend claim 22 as follows:

Claim 22, line 1 Change "21" to --20--.

REMARKS

In view of both the amendments presented above and the following discussion, the applicant submits that all of these claims now satisfy the requirements of 35 U.S.C. § 112. Thus, the applicant believes that all of these claims are now in allowable form.

Objections under 37 CFR 1.83(a)

The Examiner has objected to the drawings under 37 CFR 1.83(a) as not showing every feature of the invention specified in the claims. The applicant does not believe that such an objection is warranted, since the features that the Examiner has delineated as requiring depiction in the drawings are method steps concerning

operation of a circuit and signals that are used by the circuit. The circuitry itself is clearly depicted in the drawings in FIGs. 2(a), 2(b), 3 and 4. The applicant believes that the specification, as filed, fully describes the operation of the circuits without the need for specific drawings to the operation and signals. 37 CFR 1.83(a) does require all the features of the claims to be shown in the drawing when necessary to understand the invention. The applicant does not believe that such drawings are necessary to understanding the invention.

However, to expedite allowance of this application, the applicant is providing the requested drawings. Specifically, new FIG. 7 depicts the signals involved in the gray scale control of the EL cell including the gray scale control signal (ramp waveform and stepped waveform) of page 3, lines 57-64, the data signal as stored in the capacitor of the EL cell control circuit of page 3, line 40-43, the frame period as divided into successive LOAD and ILLUMINATE periods of page 3, line 15-17, and the current signal that is applied to the EL cell during the ILLUMINATE periods of page 4, lines 3-11. As such, comprehensive support for each of these elements that are used in gray scale control of the EL cell is found in the specification on page 3, line 15 *et seq.* and, as a result of the addition of this drawing, no new matter has been added to the specification.

New FIG. 8 depicts the signals involved in the digital gray scale control of the EL cell including the digital data signal of page 4, lines 15-16, each bit of the digital data signal is sequentially stored in the capacitor of the EL cell control circuit during the LOAD period of page 4, line 17-19, the frame period as divided into LOAD and ILLUMINATE periods of page 3, line 15-17 and page 4, lines 12-14, and the pulsed current signal that is applied to the EL cell during the ILLUMINATE periods of page 4, lines 19-33. As such, comprehensive support for each of these elements that are used in digital gray scale control of the EL cell is found in the specification on page 4, lines 12-58 and, as

a result of the addition of this drawing, no new matter has been added to the specification.

New FIGS. 7 and 8 contain all of the elements that the Examiner contends were not shown in the original figures. In view of these additional drawings, the applicant requests approval of these additional drawings and that the Examiner withdraw the objection to the drawings. Upon approval of these drawings, the applicant will file formal drawings with the Official Draftsperson.

Rejections under 35 U.S.C. § 112, first paragraph

The Examiner has rejected claims 1-16, 18-20, 25, and 27-29 under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The applicant respectfully disagrees.

As discussed above with respect to the drawing changes, the specification supports each and every claimed feature of the invention.

Specifically, in connection with gray scale control of the EL cell of claim 8, 14, and 20, the division of the frame time into LOAD and ILLUMINATE periods is discussed on page 3, lines 15-31. Subdividing a frame into LOAD and ILLUMINATE periods is also discussed on page 2, lines 35-48. During the LOAD period, the data line signal is applied to the circuit such that a transistor in the circuit applies the data signal to a capacitor for storage. See the applicant's specification on page 3, line 16-19. The applicant could not explain the storage concept during a LOAD period in any simpler terms. Those skilled in the art could easily grasp the operation of storing a data signal upon a capacitor using a transistor to apply the signal to the capacitor.

The applicant submits that the Examiner's rejection is completely inappropriate and should be withdrawn.

Similarly, the Examiner has specifically recited features of the claims from claims 9, 10, 11, 12, 14 and 20 as not being described in a manner that would allow one skilled in the art to practice the invention. The applicant believes the basis for this rejection is inappropriate. As stated above with reference to the drawing change, the specification clearly recites each and every one of the features in a manner in which any person skilled in the art would comprehend. For example, the Examiner quotes the feature of claim 9 where "said gray scale control signal has a magnitude that is less than said stored data signal" and claim 10 which recites the use of "a linear ramp waveform over the plurality of ILLUMINATION periods within one frame period." This is a simple concept that is discussed in the specification on page 3, lines 58-68 where the data signal is illustratively recited as a capacitively stored voltage of -1.5 volts and the gray scale control signal is "ramped" over the frame period from 5 volts to -5 volts. As such, the EL cell will be "on" for each ILLUMINATION period that the gray scale control signal is less than the data signal, e.g., the second transistor will not activate unless this voltage condition is present at the source and gate of the transistor. In the example given in the specification where there are 128 ILLUMINATE periods and the voltages are as stated above, the EL cell will be illuminated for 32 of the 128 ILLUMINATE periods. In claim 11, the linear ramp is replaced with a step function. The operational concept is the same. The second transistor will only turn on the EL cell when the gray scale control signal (a step function having a constant value during each ILLUMINATION period) is less than the stored data signal during any given ILLUMINATION period. Furthermore, claim 12 recites using digital bits of the data signal to directly control the gray scale level of the EL cell. The Examiner contends that the recitation in claim 12 of "a digital signal containing a plurality of bits where each bit is applied to said circuit during

a plurality of consecutive LOAD periods" is not defined in the specification such that one skilled in the art could practice the invention. The Examiner's attention is drawn to page 4, lines 12-33 where the specification describes using each bit in the digital signal (least significant bit to most significant bit) that is stored during a LOAD period to control the current applied to the EL cell during each subsequent ILLUMINATION period. For each LOAD period, a single bit is stored in a capacitive storage element, e.g., bit 0 during the first LOAD period, bit 1 during the second load period, bit 2 during the third load period, and so on. As discussed in the specification, the invention starts with the first LOAD period and the least significant bit and works up to the last LOAD period and the most significant bit. After each LOAD period, the data bit is used to control a particular number of pulses of current that are applied to the EL cell during the following ILLUMINATION period. Both the analog and digital gray scale control processes are clearly described in the specification and could easily be implemented by anyone skilled in the art. Therefore, the applicant requests that the Examiner's rejection be withdrawn.

Conclusion

Thus, the applicant submits that all of these claims now fully satisfy the requirements of 35 U.S.C. § 112. Consequently, the applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Raymond R. Moser Jr., Esq. at (908) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

Respectfully submitted,

1-16-98

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CERTIFICATE OF MAILING under 37 C.F.R. § 1.8(a)

I hereby certify that this correspondence is being deposited on January 20, 1998 with the United States Postal Service as first class mail, with sufficient postage, in an envelope addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Kathleen Fahrau
Signature

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Date of signature